## ABSTRACT OF THE DISCLOSURE

According to one embodiment, the present invention discloses a computer system that includes a memory and a memory controller. The memory controller includes a refresh timing circuit that generates clock pulses. The clock pulses are used to trigger memory refresh events. According to a further embodiment, the refresh timing circuit includes a clock generator, a counter coupled to the clock generator and a storage register coupled to the clock generator and counter. Further, the refresh timing circuit includes a comparator coupled to the clock generator, the counter and the storage register.